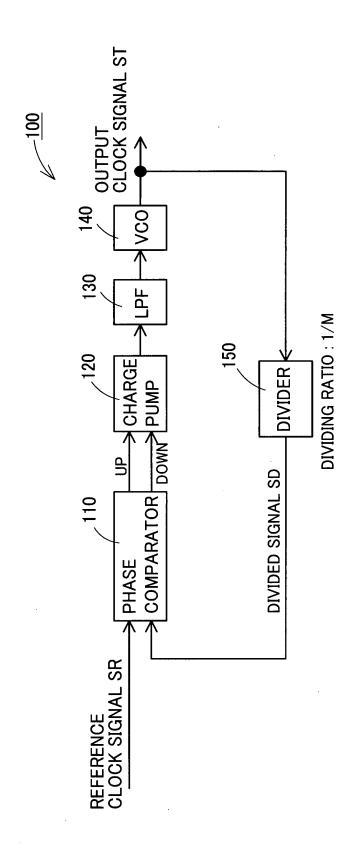
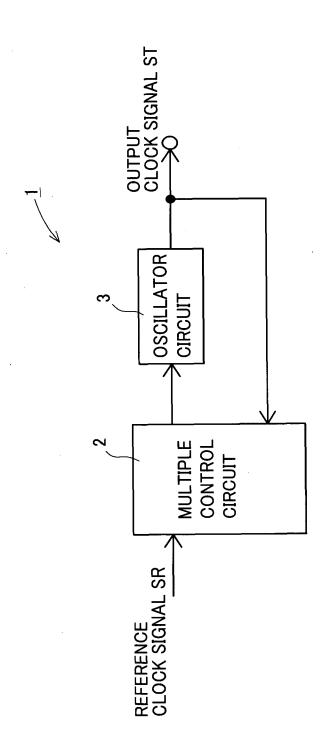
## FIG.1 PRIOR ART

BLOCK DIAGRAM SHOWING CONFIGURATION OF CONVENTONAL CLOCK CLOCK MULTIPLYING PLL CIRCUIT



BLOCK DIAGRAM ILLUSTRATING SCHEMATIC CONFIGURATION OF CLOCK MULTIPLYING PLL CIRCUIT ACCORDING TO EMBODIMENT



SDn

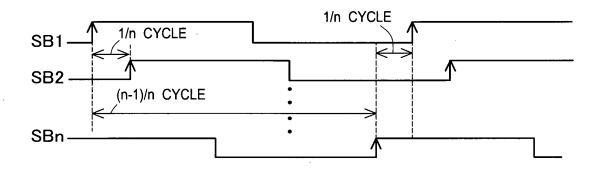
PHASE COMPARATOR SPnd

3

OUTPUT CLOCK SIGNAL BLOCK DIAGRAM DEPICTING CONFIGURATION OF CLOCK MULTIPLYING PLL 000 8 52 LPF  $\leq$ CHARGE SD2 SD1 SDOWN SUP CIRCUIT ACCORDING TO EMBODIMENT PHASE COMPARATOR SP24 PHASE COMPARATOR SP1d SP2u SB2. SB1 9 DLL REFERENCE CLOCK SIGNAL SR

## FIG.4

TIME CHART SHOWING CHANGES IN FIRST THROUGH n-th REFERENCE CLOCK SIGNAL



## FIG.5

TIME CHART ILLUSTRATING CHANGES IN FIRST THROUGH n-th DIVIDED SIGNAL

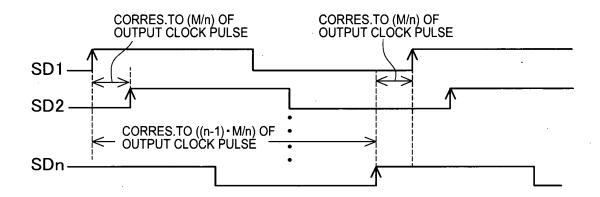
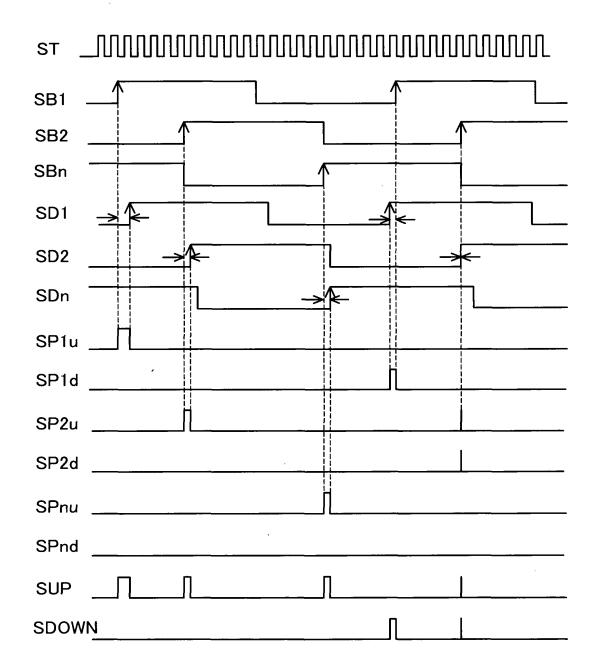


FIG.6

TIME CHART RELATED TO PHASE COMPARISONS OF CLOCK MULTIPLYING PLL CIRCUIT ACCORDING TO EMBODIMENT



ACCORDING TO EMBODIMENT AND INCLUDING DIVIDER INITIAL RESET MEANS BLOCK DIAGRAM OF CONFIGURATION OF CLOCK MULTIPLYING PLL CIRCUIT

